IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Eaton et al.

Attorney Docket No.: FULCP004X1

Application No.: 10/620,330

Examiner: Not yet assigned

Filed: July 14, 2003

Group: Not yet assigned

Title: OPTIMIZATION OF CELL SUBTYPES IN A HIERARCHICAL DESIGN FLOW

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on September 22, 2003 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____
Tara Hayden

INFORMATION DISCLOSURE STATEMENT
37 CFR §§1.56 AND 1.97(b)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

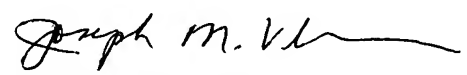
The references listed in the attached PTO Form 1449, copies of which are attached, may be material to examination of the above-identified patent application. Applicants submit these references in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make these references of official record in this application. Reference No. L is not provided because it is a U.S. Application not filed by our firm and we believe the PTO can retrieve a copy. Of course, if the Examiner would like copy of the cited reference not provided herewith, Applicant will be pleased to provide it upon request.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This Information Disclosure Statement is: (i) filed within three (3) months of the filing date of the above-referenced application, (ii) believed to be filed before the mailing date of a first Office Action on the merits, or (iii) believed to be filed before the mailing of a first Office Action after the filing of a Request for Continued Examination under §1.114. Accordingly, it is believed that no fees are due in connection with the filing of this Information Disclosure

Statement. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. FULCP004X1).

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



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Form 1449 (Modified)	Atty Docket No.	Application No.:
	FULCP004X1	10/620,330
Information Disclosure	Applicant:	
Statement By Applicant	Eaton et al.	
	Filing Date	Group
(Use Several Sheets if Necessary)	July 14, 2003	Not yet assigned

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	6,038,656	03.14.00	Martin et al.			
	B	5,752,070	05.12.98	Martin et al.			
	C	6,044,061	03.28.00	Aybay et al.			
	D	5,832,303	11.03.98	Murase et al.			

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	E	Andrew Matthew Lines, Pipelined Asynchronous Circuits, June 1995, revised June 1998, pp. 1-37.
	F	Alain J. Martin, Compiling Communicating Processes into Delay-Insensitive VLSI Circuits, December 31, 1985, Department of Computer Science California Institute of Technology, Pasadena, California, pp. 1-16.
	G	Alain J. Martin, Erratum: Synthesis of Asynchronous VLSI Circuits, March 22, 2000, Department of Computer Science California Institute of Technology, Pasadena, California, pp. 1-143.
	H	U.V. Cummings, et al. An Asynchronous Pipelined Lattice Structure Filter, Department of Computer Science California Institute of Technology, Pasadena, California, pp. 1-8.
	I	Alain J. Martin, et al. The Design of an Asynchronous MIPS R3000 Microprocessor, Department of Computer Science California Institute of Technology, Pasadena, California, pp. 1-18.
	J	C.L. Seitz, System Timing, chapter 7, pp. 218-262.
	K	F.U. Rosemberger et al., Internally Clocked Delay-Insensitive Modules, IEEE Trans., Computers, vol. 37, no. 9, pp. 1005-1018, September 1998.
	L	U.S. Application 09/501,638, filed on February 10, 2000, entitled, Reshuffled Communications Processes in Pipelined Asynchronous Circuits.
	M	Lee et al., Crossbar-Based Gigabit Packet Switch with an Input-Polling Shared Bus Arbitration Mechanism, September 21, 1997, XVI World Telecom Congress Proceedings, Interactive Session 3 – Systems Technology & Engineering, pp. 435-441.
	N	Ghosh et al., Distributed Control Schemes for Fast Arbitration in Large Crossbar Networks, March 1994, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 2, No. 1, pp. 55-67.

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.